Chip Scale Package (CSP)

Design, Materials, Processes, Reliability, and Applications

John H. Lau
Express Packaging Systems, Inc.

Shi-Wei Ricky Lee
The Hong Kong University of Science & Technology

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1.2.1 Assembly process

Figure 1.2 shows a very simplified assembly process for wire-bonding chips and solder-bumped flip chips on organic substrates. More detailed design, materials, process, reliability, and applications for wire-bonding and flip-chip technologies can be found in Ref. [1–34]. It should be noted that there are two ways to do the screening test for solder-bumped flip-chip technology. One is to test before wafer bumping. In this case, the probe marks (damages) will be on the pad, which could affect the integrity of the under-bump metallurgy and have po-

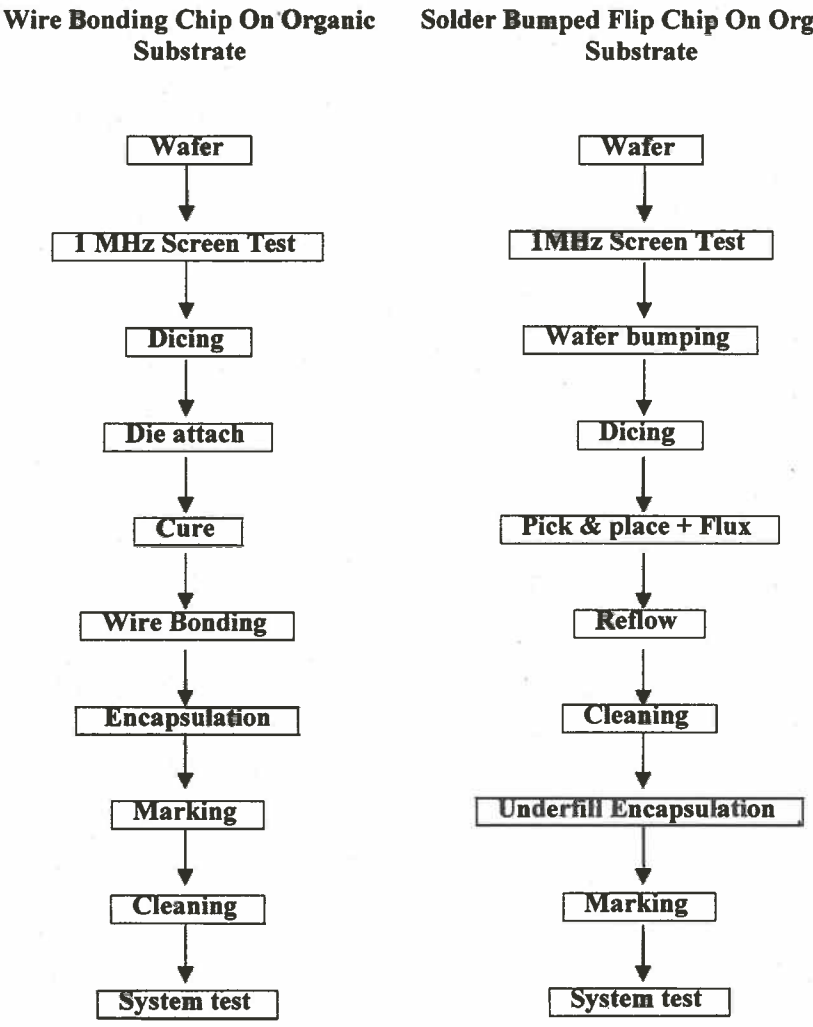

Figure 1.2 Assembly process for wire-bonding and flip-chip technologies.

tential effects on long-term reliability. The other is to test after wafer bumping. In this case, the test will contaminate the probe needles and result in shorts. Also, solder bumps may be damaged. However, better yield can be obtained because there will be better electrical contact between the probe needles and the solder bumps. For a mature wafer-bumping process, the bump yield is usually very high (>99 percent).

From a cost point of view, the most important difference between wire bonding and solder-bumped flip chip is that the wire-bonding technology needs gold wire and the solder-bumped flip-chip technology needs wafer bumping. The second most important difference between these two technologies is the effect on IC chip yields of the 1-MHz screening test and at-speed/burn-in system tests. Finally, the major equipment needed for these interconnect methods differs.

1.2.2 Major equipment

The major equipment needed by wire-bonding chips and solder-bumped flip chips on a CSP organic substrate is shown in Table 1.2. It should be noted that equipment required by both technologies is not shown. Also, all the equipment is assumed to be utilized 300 days (24 hours a day) a year, and the capacity is assumed to be 12 million chips per year.

It can be seen from Table 1.2 that expensive pick and place and fluxing machines are necessary for flip-chip technology. Even though the wire bonder is cheaper, however, because its throughput is much lower (it depends on the number of pads on a chip) than that of the pick and place machine (which performs gang bonding on a chip), more wire bonders are needed. Consequently, the cost of major equipment for flip chip ($2,700,000) is lower than that for wire bonding ($4,790,000). Also, the manufacturing floor space for flip chip should be smaller.

1.2.3 Materials/labor/operation

As mentioned earlier, the largest cost differences between wire bonding and flip chip are those for materials and IC chip yields. The labor/operation costs for these two assembly processes are assumed to be the same.

1.2.3.1 The wafer. The physically possible number of undamaged chips N_c stepped from a wafer (Fig. 1.2) may be given by

$$N_c = \pi \frac{[\phi - (1 + \theta)\sqrt{A/\theta}]^2}{4A} \tag{1.1}$$

1.3 How to Select Underfill Materials

One of the major reasons why solder-bumped flip chip on low-cost organic CSP substrates works is because of the underfill epoxy encapsulant [1–6, 10–29]. It reduces the effect of the global thermal expansion mismatch between the silicon chip and the organic substrate, i.e., it reduces the stresses and strains in the flip-chip solder bumps (since the chip and the substrate are tightly held by the underfill) and redistributes over the entire chip area the stresses and strains that would otherwise be increasingly concentrated near the corner solder bumps of the chip. Other advantages of underfill encapsulant are that it protects the chip from moisture, ionic contaminants, radiation, and hostile operating environments such as thermal [3, 5, 18], mechanical pull [3], shear [3, 22, 26–28], and twist [3, 22], and shock/vibration [24].

In this chapter, eleven different underfill encapsulants with different filler size and content and different epoxies are studied. Their curing conditions, such as time and temperature, are measured by a differential scanning calorimeter (DSC) unit. Their material properties, such as the TCE (thermal coefficient of expansion), T_g (glass transition temperature), dynamic storage modulus, tangent delta, and moisture content, are measured using thermal mechanical analysis (TMA), dynamic mechanical analysis (DMA), and thermal gravimetric analysis (TGA). Their flow rate and mechanical (shear) strength in a solder-bumped flip chip on board are measured. Their effects on the electrical performance (voltage) of a functional flip-chip device are determined experimentally. For each test configuration, the sample size is three and the values reported herein are the average.

1.3.1 Underfill materials and applications

There are eleven different encapsulant materials under consideration, namely, Underfills A, B, C, D1, D2, D3 (three different lots), E, F, G, H, and I (Table 1.4). All of the underfill encapsulants are premixed at the supplier sites, packed in plastic syringes (5 to 10 mL), and then frozen packed at −40°C to prevent curing. In shipping, these underfill materials require special handling to maintain the low temperature continuously. Upon receiving the package, one needs to unpack the package, take out the syringes quickly, and store them in a freezer at an uninterrupted temperature of −40°C. Under these conditions, most of the underfill encapsulants would have approximately one year storage life.

The filler content and size for Underfills A, B, C, D1, D2, D3, E, F, G, H, and I are shown in Table 1.4. For all these underfills, the filler is silica. The resin of Underfills A, B, C, D1, D2, and D3 is bisphenol-type epoxy; that of Underfill H is a mixture of bisphenol epoxy and a